Zihao (Harry) Liu

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EDUCATION

University of Edinburgh — **Edinburgh, United Kingdom**
Master's Degree in High Performance Computing — *Sep. 2023 – Aug. 2024*

- Member of TeamEPCC - Participated in the International Supercomputing Conference (ISC) Student Cluster Competition (SCC), held in Germany at May 2024.
- **Grade**: Merit

University of Bristol — **Bristol, United Kingdom**
Bachelor's Degree in Electrical and Electronic Engineering — *Sep. 2019 – Jun. 2023*

- **Grade:** Second Class Honours (First Division).

WORK EXPERIENCES

Arm — **Manchester, United Kingdom**
Graduate Engineer (Rotation within System MMU team) — *Sep. 2024 – Present*

- **RTL Design Role**
  - Redesigned shared RTL modules, including parity-protected registers and custom delay reset-sampling logic.
  - Verified correctness with designer SVA assertions and Formality LEC.
  - Performed synthesis using standard-cell libraries with different voltage thresholds and analyzed timing/area trade-offs to determine achievable frequency and identify critical-path bottlenecks.
  - Exposure to low-power techniques including state-retention and clock-gating strategies while participating in cache microarchitecture design meetings.
  - Developed a module instantiation analysis Python tool to scan the codebase and report port/parameter usage in each instantiation of the same module. Analysed parameter usage and removed redundant parameters.
  - Created three JasperGold custom linting rules using TCL to flag non-compliant coding patterns.
  - Updated standard RTL components (e.g. logic gates, n-depth synchroniser, clock-gating cells) in SMMU to align with Arm-wide design conventions, gaining exposure to CDC methodologies and standardized design practices.
- **Formal Verification Role**
  - Designed and brought up three formal testbenches from scratch for previously unverified blocks in SMMU and discovered 14 functional RTL bugs that dynamic verification missed.
  - Independently root-caused failing formal properties, identifying underlying RTL issues before handing-off to designers, reducing designer debug time.
  - Maintained and stabilized two inherited formal testbenches, cleaning unreachable properties, resolving over-constraints, and improving abstraction models for complex data and control paths.
  - Familiar with formal techniques including bounded coverage analysis, COI/Proofcore coverage analysis, X-propagation checking and proof-depth tuning.
  - Integrated formal testbenches with dynamic simulations, debugging and resolving over-constrained properties to ensure formal models accurately reflect hardware behavior.
- **Additional Responsibilities**
  - Served as internal Out-of-Box reviewer for three product release sign-offs. Reviewed documentation, installation flows, and testbench usage guides to improve clarity before customer delivery.

Huawei Technologies Research & Development (UK) Ltd — **Edinburgh, United Kingdom**
Research Intern — *Apr. 2024 – Aug. 2024*

- Developed a Python-based Gem5 checkpointing tool that extracts hardware simulation statistics such as TLB and cache hits, memory access latency, and bandwidth to support CPU memory management research.
- Generated checkpoints using simple CPU models after launching client-server applications (Redis, MySQL) in Gem5, enabling researchers to restore checkpoints with complex CPU models for simulations that provide more fine-grained statistics.
- Enhanced the tool to parallelize the restoration of multiple checkpoints and automate launching multiple Gem5 simulations with a variety of boot configuration and set-ups.
- Worked on restoring QEMU-based checkpoints using Gem5 CPU models.
- Created Linux root file systems, disk images, and kernels for both QEMU and Gem5 environments.

Arm **Manchester, United Kingdom**

Hardware Engineering Intern *Jul. 2023 – Mar. 2024*

- Interned with the System Memory Management Unit (SMMU) Design Team.
- Contributed to a Python-based register generation workflow that automatically produces RTL design for configuration register host blocks and corresponding UVM coverage file, eliminating redundant and error-prone manual coding for register verification.
- Developed four reusable SystemVerilog templates that can be fed into the workflow to generate RTL for 40+ register host blocks, along with coverpoints using various bin types and cross coverage to ensure all register values are exercised.
- Developed a new feature that enables designer adding custom register field guarding conditions that can be picked up by the flow and incorporate into RTL.
- Refactored part of the flow which reduced auto-generation time by at least 20%.
- Participated in technical design and timing review discussions, gaining exposure to industry-standard best practices.

Huawei Technologies Research & Development (UK) Ltd **Cambridge, United Kingdom**

Research Intern *Feb. 2023 – Jun. 2023*

- Designed and implemented CI/CD pipelines from scratch for the Team using GitLab CI and Jenkins.
- Improved computational resource efficiency by deploying a Kubernetes machine cluster for running regression jobs.
- Built and customized Docker images for multiple test environments and integrated them into the Kubernetes cluster.
- Developed Jenkins pipelines for nightly, merge requests, and sanity regressions, and utilized Jenkins plugins for cross-pipeline triggering and automated email notifications.
- Created a Python-based test report generation tool with Pandas to parse LLVM testsuite logs, delivering visualized regression statistics via a variety of charts and graphs.

SKILLS & INTERESTS

Skills: English (Fluent), Chinese (Native), SystemVerilog, SVA, RTL Design, Formal Verification, Python, C, Linux, Git, Jenkins, CI/CD, TCL

Interests: Badminton, Football, Volleyball, Hiking, Board Games, League of Legends